CLAIMS

1-24. (Canceled)

25. (Previously Presented) A programmable processor for executing a plurality of programs, said programmable processor comprising:

a target program counter coupled to a plurality of program counters, said target program counter for determining a number of programs to interleave from a plurality of programs that is greater than the number of program counters;

each of said plurality of program counters coupled to an instruction memory;

instructions from said instruction memory coupled to an instruction decode;

said decode coupled to a plurality of registers;

each of said plurality of registers coupled to an operand route;

said operand route coupled to an arithmetic datapath;

said datapath and an output of a data memory coupled to a result route; and

an output of said result route fed back to each of said plurality of registers.

26. (Previously Presented) The programmable processor of claim 25 wherein said plurality of program counters is equal to said plurality of programs to be interleaved.

27. (Previously Presented) The programmable processor of claim 25 wherein said plurality of registers is equal to said plurality of programs to be interleaved.

28. (Previously Presented) The programmable processor of claim 25 wherein said plurality of registers is more than said plurality of programs to be interleaved.

29. (Previously Presented) The programmable processor of claim 25 wherein said instruction memory is larger than needed to hold said plurality of programs.

30. (Previously Presented) The programmable processor of claim 25 wherein said data memory is larger than needed to hold a data set accessed by each of said plurality of programs.

31. (Previously Presented) The programmable processor of claim 25 wherein each of said plurality of registers is double buffered and contains twice as many copies of registers as said plurality of programs.

32. (Canceled)

33. (Canceled)